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12EC009

M.Tech. Degree Examination, Dec.2014/Jan.2015

Advances in VLSI Design

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions.***

1 a. Explain in detail BiCMOS fabrication in n-well process. **(08 Marks)**

b. Compare CMOS and Bipolar technologies. **(04 Marks)**

c. Explain the following forms of an inverter circuit if pull up transistor is replaced by:
   i) Load resistor
   ii) CMOS pull up
   iii) n-MOS enhancement transistor
   iv) n-MOS depletion mode transistor **(08 Marks)**

2 a. Explain JFET device and its V-I characteristics for:
   i) Zero gate bias applied
   ii) Non-zero gate bias applied **(10 Marks)**

b. With the help of a band diagram, explain the basic principle of modulation doping and also the operation of a HEMT device formed with GaAS/GaAℓAs. **(10 Marks)**

3 a. A JFET has $N_a = 10^{19}/cm^3$, $N_d = 10^{16}/cm^3$, a = 0.1μm, L = 10 μm and Z = 1 mm. Assume the device is S_i with $N_i = 10^{10}/cm^3$ and a relative dielectric constant of 11.8. Assume also that in saturation the square law can be used and that the value of I_{DO} is 5.0 μA. Determine the following:
   i) The built-in voltage
   ii) The pinch of voltage
   iii) The drain saturation voltage if $V_G = -2V$.
   iv) The drain current if $V_D = 1V$ and the gate bias is -2V. **(10 Marks)**

b. Draw and explain the energy band diagram of an MIS structure under:
   i) Forward bias
   ii) Low reverse bias
   iii) High reverse bias **(10 Marks)**

4 a. Quantitatively determine the relationship between I_D, V_{GS} and V_D under different biasing conditions for MOSFET device. **(10 Marks)**

b. Consider an n-channel Si MOSFET with the following information:
$V_T = 2V$, oxide thickness d = 0.1 nm, $\mu_n^l = 500\ cm^2/VS$, Z = 10 μm, L = 10 μm.
Calculate the drain current assuming the gate voltage is $V_G = 6V$ and that the drain voltage is (i) 1V and (ii) 6V. **(10 Marks)**

5 a. With suitable mathematical analysis describe the short channel effects as applied to V_T reduction and surface mobility in a MOSFET. **(10 Marks)**

b. Bring out the difference between constant field, constant voltage and quasi constant voltage scaling methods. **(04 Marks)**

c. Explain the working principle of carbon nanotubes. **(06 Marks)**

6 a. What do you mean by defect tolerant computing? **(04 Marks)**

b. What is the need for super buffers? Explain NMOS inverting and non inverting super buffers with the help of schematic and stick diagrams. **(10 Marks)**

c. Explain the working of a BiCMOS inverter with relevant circuit diagram in which problems associated with stored charge in the base of non conducting transistors (BJT). How the problem can be prevented? **(06 Marks)**

7 a. What are the major rules associated while designing NMOS pass transistor logic? Highlight any two advantages of pass transistor logic. **(05 Marks)**

b. Draw the circuit, stick diagram for CMOS transmission gate. **(05 Marks)**

c. Explain the conceptual approach in designing a tally circuit with the help of tree network. **(10 Marks)**

8 a. Explain the terms hierarchy, regularity, modularity and locality as applied to structured design strategies. **(10 Marks)**

b. Write explanatory notes on:

i) Local routing using line-search approach.

ii) Standard cell based design. **(10 Marks)**

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